

HETEROJUNCTION FIELD EFFECT TYPE SEMICONDUCTOR DEVICE  
HAVING HIGH GATE TURN-ON VOLTAGE AND LOW ON-RESISTANCE  
AND ITS MANUFACTURING METHOD

5 BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a heterojunction field effect type semiconductor device and its manufacturing method.

10 Description of the Related Art

Generally, in a transmitter of a mobile handset, a power amplifier has been required to operate at a lower voltage and have a lower ON-resistance. A GaAs heterojunction field effect type semiconductor device is used as such a power amplifier.

In a first prior art GaAs heterojunction field effect type semiconductor device (see: Yasunori BITO et al., Fig. 2 of "64% Efficiency Enhancement-Mode Power Heterojunction FET for 3.5V Li-Ion Battery Operated Personal 20 Digital Cellular Phones", 1998 IEEE MTT-S Int. Microwave Symp-Dig., pp. 439-442, June 1998), a channel layer, an undoped AlGaAs Schottky layer, an undoped GaAs layer and a Si-doped n<sup>+</sup>-type cap layer are sequentially grown by an epitaxial growth process, and a double-recess structure is 25 provided in the Si-doped n<sup>+</sup>-type cap layer and the undoped GaAs Schottky layer. Then, a gate electrode is formed on the undoped AlGaAs Schottky layer via the double-recess structure, and an ohmic source electrode and an ohmic drain electrode are formed on the Si-doped n<sup>+</sup>-type cap layer. This will be explained later 30 in detail.

In the above-described first prior art GaAs field effect type semiconductor device, since the double-recess structure is adopted, the ON-resistance can be decreased.

In the above-described first prior art GaAs field effect type semiconductor device, however, since the gate electrode is in direct contact with the undoped AlGaAs Schottky layer, the effective Schottky barrier therebetween 5 is so small, i.e., about 1.0eV that the gate turn-on voltage  $V_f$  is small, i.e., about 0.7V. Therefore, in a normal operation, the gate electrode is forwardly turned ON to create a gate current leakage.

In a second prior art GaAs heterojunction field 10 effect type semiconductor device (see: Shigeki WADA et al., "0.1- $\mu$ m p<sup>+</sup>-GaAs Gate HJFET's Fabricated Using Two-Step Dry-Etching and Selective MMBE Growth Techniques", IEEE Transactions on Electron Devices, Vol. 45, No.6, pp. 1383-1389, June 1998), a channel layer, an undoped AlGaAs Schottky layer 15 and a Si-doped n<sup>+</sup>-type cap layer are sequentially grown by a first epitaxial growth process, and a recess structure is provided in the Si-doped n<sup>+</sup>-type cap layer. Then, a carbon-doped p<sup>+</sup>-type GaAs layer is grown on the undoped AlGaAs Schottky layer by a second epitaxial growth process. Then, a 20 gate electrode is formed on the carbon-doped p<sup>+</sup>-type AlGaAs Schottky layer, and an ohmic source electrode and an ohmic drain electrode are formed on the Si-doped n<sup>+</sup>-type cap layer. This also will be explained later in detail.

In the above-described second prior art GaAs 25 heterojunction field effect type semiconductor device, since the carbon-doped p<sup>+</sup>-type GaAs layer forms a p<sup>+</sup>-n junction with its underlaying layers, an effective Schottky barrier against electrons within a channel formed in the undoped InGaAs channel layer is substantially increased. That is, this 30 effective Schottky barrier is increased to a degree of the bandgap of the carbon-doped p<sup>+</sup>-type GaAs layer such as 1.4eV.

In the above-described second prior art GaAs field effect type semiconductor device, however, although the

effective Schottky barrier is increased from about 1.0eV to about 1.4eV by about 0.4eV as compared with the above-described first prior art GaAs field effect type semiconductor device, the gate turn-on voltage  $V_f$  is increased  
5 from about 0.7V to about 0.9V by only about 0.2V as compared with the above-described first prior art GaAs field effect type semiconductor device due to the direct contact of the carbon-doped p<sup>+</sup>-type GaAs layer with the undoped AlGaAs Schottky layer. Therefore, in a normal operation, the gate  
10 electrode is still forwardly turned ON to create a gate leakage current.

In a third prior art GaAs heterojunction field effect type semiconductor device (see: K. NISHI et al., "High Current/gm self-Alignment PJ-HFET of Completely  
15 Enhancement-Mode Operation", Extended Abstracts of the 1998 International Conference on Solid-State Devices and Materials, pp. 396-397, 1998), a channel layer, an undoped AlGaAs Schottky layer, an undoped GaAs Schottky layer and a carbon-doped p<sup>+</sup>-type GaAs layer are sequentially grown at an  
20 epitaxial growth process. Also, a gate electrode is formed on the carbon-doped p<sup>+</sup>-type GaAs layer. Further, n<sup>+</sup>-type contact regions, and an ohmic source electrode and an ohmic drain electrode are formed on the n<sup>+</sup>-type contact regions. This also will be explained later in detail.

25 In the above-described third prior art GaAs heterojunction field effect type semiconductor device, no defects are induced in the epitaxially grown carbon-doped p<sup>+</sup>-type GaAs layer, so that the gate turn-on voltage  $V_f$  can be increased to about 1.12V by about 0.22V as compared with  
30 the above-described second prior art GaAs heterojunction field effect type semiconductor device.

In the above-described third prior art GaAs field effect type semiconductor device, however, the ON-resistance

is large, which will be explained in detail.

#### SUMMARY OF THE INVENTION

It is an object of the present invention to a  
5 heterojunction field effect type semiconductor device having  
a high gate turn-on voltage and a low ON-resistance.

According to the present invention, in a  
heterojunction field effect type semiconductor device, a  
channel layer is formed over a GaAs substrate, and a first  
10 semiconductor layer including no aluminum is formed over the  
channel layer. First and second cap layers of a first  
conductivity type are formed on the first semiconductor layer,  
to create a recess on the first semiconductor layer. First and  
second ohmic electrodes are formed on the first and second cap  
15 layers, respectively. A second semiconductor layer of a second  
conductivity type is formed on the first semiconductor layer  
within the recess, and the second semiconductor layer is  
isolated from the first and second cap layers. A gate electrode  
is formed on the second semiconductor layer.

20 Also, in a method for manufacturing a  
heterojunction field effect type semiconductor device, at  
least a channel layer, a first semiconductor layer having no  
aluminum, a wide recess etching stopper layer of a first  
conductivity type, and a cap layer of the first conductivity  
25 type are grown over a GaAs substrate by a first epitaxial  
growth process. Then, the cap layer is selectively removed by  
using the wide recess etching stopper layer as a stopper to  
create a recess within the cap layer. Then, an insulating layer  
made of SiO<sub>2</sub> or the like is deposited on the entire surface.  
30 Then, the insulating layer is perforated to expose the first  
semiconductor layer. Then, a second semiconductor layer of a  
second conductivity type is grown by a second epitaxial growth  
process, so that the second semiconductor layer is buried in

the recess and contacts the first semiconductor layer. Then, a gate electrode is formed on the second semiconductor layer. Finally, ohmic electrodes are formed on the cap layer.

## 5 BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description set forth below, as compared with the prior art, with reference to the accompanying drawings, wherein:

10 Fig. 1 is a cross-sectional view illustrating a first prior art GaAs heterojunction field effect type semiconductor device;

Fig. 2 is a cross-sectional view illustrating a second prior art GaAs heterojunction field effect type semiconductor  
15 device;

Fig. 3 is a cross-sectional view illustrating a third prior art GaAs heterojunction field effect type semiconductor device;

Fig. 4 is a cross-sectional view illustrating a first  
20 embodiment of the GaAs heterojunction field effect type semiconductor device according to the present invention;

Figs. 5A through 5H are cross-sectional views for explaining a method for manufacturing the GaAs heterojunction field effect type semiconductor device of Fig. 4;

25 Figs. 6 and 7 are cross-sectional views illustrating first and second modifications of the GaAs heterojunction field effect type semiconductor device of Fig. 4;

Fig. 8 is a cross-sectional view illustrating a second embodiment of the GaAs heterojunction field effect type  
30 semiconductor device according to the present invention;

Fig. 9A is a graph showing the gate recess depth characteristics of the device of Fig. 8;

Fig. 9B is a graph showing the gate breakdown

voltage-to-maximum drain current characteristics of the device of Fig. 8;

Figs. 10A through 10J are cross-sectional views for explaining a method for manufacturing the GaAs heterojunction field effect type semiconductor device of Fig. 8; and

Figs. 11, 12, 13, 14, 15, 16, 17 and 18 are cross-sectional views illustrating first, second, third, fourth, fifth, sixth, seventh and eighth modifications of the GaAs heterojunction field effect type semiconductor device of Fig. 8.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the description of the preferred embodiments, prior art GaAs heterojunction field effect type semiconductor devices (transistors) will be explained with reference to Figs. 1, 2 and 3.

In Fig. 1, which illustrates a first prior art GaAs heterojunction field effect type semiconductor device (see: Yasunori BITO et al., Fig. 2 of "64% Efficiency Enhancement-Mode power Heterojunction FET for 3.5V Li-Ion Battery Operated Personal Digital Cellular Phones", 1998 IEEE MTT-S Int. Microwave Symp-Dig., pp. 439-442, June 1998), reference numeral 1 designates a semi-insulating GaAs substrate. Also, an undoped AlGaAs buffer layer 2, an Si-doped n<sup>+</sup>-type AlGaAs electron supply layer 3, an undoped AlGaAs spacer layer 4, an undoped InGaAs channel layer 5, an undoped AlGaAs spacer layer 6, a Si-doped n<sup>+</sup>-type AlGaAs electron supply layer 7, an undoped AlGaAs Schottky layer 8, an undoped GaAs Schottky layer 9, a Si-doped n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 and a Si-doped n<sup>+</sup>-type GaAs cap layer 11 are sequentially grown on the GaAs substrate 1 by an epitaxial growth process. Also, an insulating layer 12 made of silicon dioxide is formed on the undoped GaAs Schottky layer

9. Further, a gate electrode 13 made of aluminum or the like is formed on the undoped AlGaAs Schottky layer 8 via a recess within the undoped GaAs layer 9. Additionally, an ohmic source electrode 14S and an ohmic electrode 14D made of AuGe/Au or  
5 the like are formed on the Si-doped n<sup>+</sup>-type GaAs cap layer 11.

In the GaAs heterojunction field effect type semiconductor device of Fig. 1, since a double recess structure is adopted, the ON-resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D can be  
10 decreased.

In the GaAs field effect type semiconductor device of Fig. 1, however, since the gate electrode 13 is in direct contact with the undoped AlGaAs Schottky layer 8, the effective Schottky barrier therebetween is so small, i.e., about 1.0eV that the gate turn-on voltage V<sub>f</sub> is small, i.e., about 0.7V. Therefore, in a normal operation, the gate electrode 13 is forwardly turned ON to create a gate leakage current.  
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Note that a gate turn-on voltage is defined when a  
20 gate current leakage is 1mA/mm.

In Fig. 2, which illustrates a second prior art GaAs heterojunction field effect type semiconductor device (see: Shigeki WADA et al., "0.1-μm p<sup>+</sup>-GaAs Gate HJFET's Fabricated Using Two-Step Dry-Etching and Selective MOCVD Growth Techniques", IEEE Transactions on Electron Devices, Vol. 45, No.6, pp. 1383-1389, June 1998), reference numeral 201 designates a semi-insulating GaAs substrate. Also, an undoped AlGaAs buffer layer 202, an Si-doped n-type AlGaAs electron supply layer 203, an undoped InGaAs channel layer 204, a  
25 Si-doped n-type AlGaAs electron supply layer 205, an undoped AlGaAs Schottky layer 206, and a Si-doped n<sup>+</sup>-type GaAs cap layer 207 are sequentially grown on the GaAs substrate 201 by a first epitaxial growth process. Also, an insulating layer  
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208 made of silicon dioxide is formed on the undoped AlGaAs Schottky layer 206. Further, a carbon-doped p<sup>+</sup>-type GaAs layer 209 is grown on the undoped AlGaAs Schottky layer 206 via a recess within the insulating layer 208 by a second  
5 epitaxial growth process. Additionally, a gate electrode 210 made of aluminum or the like is formed on the carbon-doped p<sup>+</sup>-type GaAs layer 209. Further, an ohmic source electrode 211S and an ohmic drain electrode 211D made of AuGe/Au or the like are formed on the Si-doped n<sup>+</sup>-type GaAs cap layer 207.  
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In the GaAs heterojunction field effect type semiconductor device of Fig. 2, since the carbon-doped p<sup>+</sup>-type GaAs layer 209 forms a p<sup>+</sup>-n junction with its underlaying layers, an effective Schottky barrier against electrons within a channel formed in the undoped InGaAs channel layer  
15 204 is substantially increased. That is, this effective Schottky barrier is increased to a degree of the bandgap of the carbon-doped p<sup>+</sup>-type GaAs layer 209 such as 1.4eV.

In the GaAs field effect type semiconductor device of Fig. 2, however, although the effective Schottky barrier  
20 is increased from about 1.0eV to about 1.4eV by about 0.4eV as compared with the GaAs field effect type semiconductor device of Fig. 1, the gate turn-on voltage V<sub>f</sub> is increased from about 0.7V to about 0.9V by only about 0.2V as compared with the GaAs field effect type semiconductor device of Fig. 1.  
25 Therefore, in a normal operation, the gate electrode 210 is still forwardly turned ON to create a gate leakage current.

The reason why the gate turn-on voltage V<sub>f</sub> is not so increased is that the carbon-doped p<sup>+</sup>-type GaAs layer 209 is epitaxially grown directly on the undoped AlGaAs Schottky  
30 layer 206. That is, the undoped AlGaAs Schottky layer 206 is exposed to the air, the aluminum component of the undoped AlGaAs Schottky layer 206 actively reacts with oxygen so that aluminum oxide is created thereon. Since the aluminum oxide

is difficult to be removed, the aluminum oxide induces defects in the epitaxially-grown carbon-doped p<sup>+</sup>-type GaAs layer 209, so that the gate turn-on voltage V<sub>f</sub> is decreased to create a gate leakage current.

5        In Fig. 3, which illustrates a third prior art GaAs heterojunction field effect type semiconductor device (see: K. NISHI et al., "High Current/gm self-Alignment PJ-HFET of Completely Enhancement-Mode Operation", Extended Abstracts of the 1998 International Conference on Solid-State Devices 10 and Materials, pp. 396-397, 1998), reference numeral 301 designates a semi-insulating GaAs substrate. Also, an undoped AlGaAs buffer layer 302, an Si-doped n<sup>+</sup>-type AlGaAs electron supply layer 303, an undoped AlGaAs spacer layer 304, an undoped InGaAs channel layer 305, an undoped AlGaAs spacer 15 layer 306, a Si-doped n<sup>+</sup>-type AlGaAs electron supply layer 307, an undoped AlGaAs Schottky layer 308, an undoped GaAs Schottky layer 309 and a carbon-doped p<sup>+</sup>-type GaAs layer 310 are sequentially grown on the GaAs substrate 301 by an epitaxial growth process. Also, a gate electrode 311 made of WSi or the 20 like is formed on the carbon-doped p<sup>+</sup>-type GaAs layer 310. Further, n<sup>+</sup>-type contact regions 312S and 312D are formed in the substrate 301 and the layers 302 through 309 by an implantation of Si in self-alignment with the gate electrode 311 and the carbon-doped p<sup>+</sup>-type GaAs layer 310. In this case, 25 the gate electrode 311 and the carbon-doped p<sup>+</sup>-type GaAs layer 310 are larger than those as illustrated in Fig. 3. After the gate electrode 311 and the carbon-doped p<sup>+</sup>-type GaAs layer 310 are further reduced by an etching process as illustrated in Fig. 3, an ohmic source electrode 313S and an ohmic drain 30 electrode 313D made of AuGe/Au or the like are formed on the n<sup>+</sup>-type contact regions 312S and 312D, respectively.

      In the GaAs heterojunction field effect type semiconductor device of Fig. 3, the carbon-doped p<sup>+</sup>-type GaAs

layer 310 as well as the other layers 302 through 309 is grown in the same epitaxial growth process, and the carbon-doped p<sup>+</sup>-type GaAs layer 310 is not in contact with the undoped AlGaAs Schottky layer 308, there is no oxide at the bottom of 5 the carbon-doped p<sup>+</sup>-type GaAs layer 310, so that no defects are induced in the epitaxially grown carbon-doped p<sup>+</sup>-type GaAs layer 310, thus increasing the gate turn-on voltage V<sub>f</sub> to about 1.12V by about 0.22V as compared with the GaAs heterojunction field effect type semiconductor device of Fig. 2.

10 In the GaAs field effect type semiconductor device of Fig. 3, however, the ON-resistance between the ohmic source electrode 313S and the ohmic drain electrode 313D is large. That is, since the ohmic source electrode 313S and the ohmic drain electrode 313D are connected to the n<sup>+</sup>-type contact 15 regions 312S and 312D, respectively, the contact resistances therebetween are large which would increase the ON-resistance. Also, since the distance between a channel created in the undoped InGaAs channel layer 305 and the surface of the undoped GaAs Schottky layer 309 is small, the concentration of sheet 20 carriers in the channel is decreased by the surface depletion region of the undoped InGaAs GaAs Schottky layer 309, so that the sheet resistance of a region between the gate electrode 311 and the n<sup>+</sup>-type contact regions 312S and 312D is large, which also would increase the ON-resistance. Particularly 25 when the GaAs field effect type semiconductor device of Fig. 3 is applied to an enhancement type field effect transistor having a positive threshold voltage, since the distance between the carbon-doped p<sup>+</sup>-type GaAs layer 310 and the above-mentioned channel is further decreased, the 30 concentration of sheet carriers in the channel is further decreased, so that the above-mentioned sheet resistance per unit area is several thousands of Ω. Thus, the GaAs field effect type semiconductor device of Fig. 3 cannot be applied

to mobile handsets operating at a low voltage such as 3V.

In Fig. 4, which illustrates a first embodiment of the GaAs heterojunction field effect type semiconductor device according to the present invention, a carbon-doped 5 p<sup>+</sup>-type GaAs layer 15 corresponding to the carbon-doped p<sup>+</sup>-type GaAs layer 209 of Fig. 2 is added to the elements of Fig. 1. Also, the carbon-doped p<sup>+</sup>-type GaAs layer 15 is in contact with the undoped GaAs Schottky layer 9, not the undoped AlGaAs Schottky layer 8.

10 Since the carbon-doped p<sup>+</sup>-type GaAs layer 15 is not in contact with the undoped AlGaAs Schottky layer 8 whose aluminum component is easily oxidized, the gate turn-on voltage V<sub>f</sub> can be increased to about 1.2V.

Also, in a similar way to in the GaAs heterojunction 15 field effect type semiconductor device of Fig. 1, the ON-resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D can be small, i.e., about 2Ω · mm.

A method for manufacturing the GaAs heterojunction field effect type semiconductor device of Fig. 4 will be 20 explained next with reference to Figs. 5A through 5H.

First, referring to Fig. 5A, an about 50nm thick undoped AlGaAs buffer layer 2, an about 4nm thick n<sup>+</sup>-type AlGaAs electron supply layer 3 having about  $3 \times 10^{18}$  Si atoms cm<sup>-3</sup> doped therein, an about 2nm thick undoped AlGaAs spacer 25 layer 4, an about 15nm thick undoped InGaAs channel layer 5, an about 2nm thick undoped AlGaAs spacer layer 6, an about 9nm thick n<sup>+</sup>-type AlGaAs electron supply layer 7 having about  $3 \times 10^{18}$  Si atoms cm<sup>-3</sup> doped therein, an about 7nm thick AlGaAs Schottky layer 8, an about 5nm thick undoped GaAs Schottky 30 layer 9, an about 5nm thick n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 having about  $4 \times 10^{18}$  Si atoms cm<sup>-3</sup> doped therein and an about 100nm thick n<sup>+</sup>-type GaAs cap layer 11 having  $4 \times 10^{18}$  Si atoms cm<sup>-3</sup> doped therein are sequentially

grown on a semi-insulating GaAs substrate 1 by a first epitaxial growth process using a molecular beam epitaxy (MBE) method or a metalorganic vapor phase epitaxy (MOVPE) method.

Next, referring to Fig. 5B, a photoresist pattern 21 is formed by a photolithography process. Then, the n<sup>+</sup>-type GaAs cap layer 11 is etched by a dry etching process using the photoresist pattern 21 as a mask and the n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 as a stopper. In this case, a part of the n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 is also etched. Thus, a wide recess 11a is created in the n<sup>+</sup>-type GaAs cap layer 11.

Next, referring to Fig. 5C, the remainder of the n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 is completely removed by a rinsing process. Then, the photoresist pattern 21 is removed. Thus, the wide recess 11a is further increased to create a wide recess 10a.

Next, referring to Fig. 5D, an insulating layer 12 made of silicon dioxide is deposited on the entire surface by a chemical vapor deposition (CVD) process.

Next, referring to Fig. 5E, a photoresist pattern 22 is formed by a photolithography process. Then, the insulating layer 12 is etched by an etching process using the photoresist pattern 22 as a mask. As a result, the undoped GaAs Schottky layer 9 is exposed. Then, the photoresist pattern 22 is removed.

Next, referring to Fig. 5F, an about 80nm thick carbon-doped p<sup>+</sup>-type GaAs layer 15 having about  $1 \times 10^{20}$  carbon atoms cm<sup>-3</sup> doped therein is selectively grown on the exposed undoped GaAs Schottky layer 9 by a second epitaxial growth process using an MOVPE method.

Next, referring to Fig. 5G, a gate electrode 13 made of WSi is formed by a sputtering process. Then, the gate electrode 13 is patterned by a photolithography and etching

process.

Next, referring to Fig. 5H, the insulating layer 12 is further patterned by a photolithography and etching process. Thus, the n<sup>+</sup>-type GaAs layer 11 is exposed.

5 Finally, returning to Fig. 4, an ohmic layer made of AuGe is deposited on the exposed n<sup>+</sup>-type GaAs cap layer 11 by an evaporation and lift-off process. Then, the ohmic layer is alloyed and patterned by a photolithography and etching process. Thus, an ohmic source electrode 14S and an ohmic drain  
10 electrode 14D are formed.

In Fig. 6, which illustrates a first modification of the GaAs heterojunction field effect semiconductor device of Fig. 4, the Si-doped n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 of Fig. 4 is replaced by a Si-doped n<sup>+</sup>-type  
15 InGaP wide recess etching stopper layer 10'. Even in the GaAs heterojunction field effect semiconductor device of Fig. 6, the gate turn-on voltage V<sub>f</sub> can be increased to about 1.2V. Also, the ON-resistance can be small, i.e., about 2Ω · mm.

In Fig. 7, which illustrates a second modification  
20 of the GaAs heterojunction field effect semiconductor device of Fig. 4, the Si-doped n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 of Fig. 4 is replaced by a Si-doped n<sup>+</sup>-type InGaP wide recess etching stopper layer 10''. The carbon-doped p<sup>+</sup>-type GaAs layer 15 is in contact with the Si-doped n<sup>+</sup>-type  
25 InGaP wide recess etching stopper layer 10'' that does not include aluminum which is easily oxidized. Even in the GaAs heterojunction field effect semiconductor device of Fig. 7, the gate turn-on voltage V<sub>f</sub> can be increased to about 1.2V. Also, the ON-resistance can be small, i.e., about 2Ω · mm.

30 When manufacturing the GaAs heterojunction field effect type semiconductor device of Fig. 7, since the complete removing process of the Si-doped n<sup>+</sup>-type InGaP wide recess etching stopper layer 10'' is unnecessary, the manufacturing

steps therefor can be simplified.

In Fig. 8, which illustrates a second embodiment of the GaAs heterojunction field effect type semiconductor device according to the present invention, an undoped AlGaAs gate recess stopper layer 16 and an undoped GaAs layer 17 are added to the elements of the GaAs heterojunction field effect type semiconductor device of Fig. 4, and the carbon-doped p<sup>+</sup>-type GaAs layer 15 is formed on the undoped GaAs Schottky layer 9 through a gate recess provided in the undoped AlGaAs gate recess stopper layer 16 and the undoped GaAs layer 17.

In the same way as in the GaAs heterojunction field effect type semiconductor device of Fig. 4, since the carbon-doped p<sup>+</sup>-type GaAs layer 15 is not in contact with the undoped AlGaAs Schottky layer 8 whose aluminum component is easily oxidized, the gate turn-on voltage V<sub>f</sub> can be increased to about 1.2V. Also, in a similar way to the GaAs heterojunction field effect type semiconductor device of Fig. 1, the ON-resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D can be small, i.e., about 1.6 Ω · mm. Also, the mutual conductance is increased to about 470 mS/mm.

Further, since the carbon-doped p<sup>+</sup>-type GaAs layer 15 is partly buried in the gate recess in the undoped AlGaAs gate recess etching stopper layer 16 and the undoped GaAs layer 17, the sheet resistance around the wide recess in the Si-doped n<sup>+</sup>-type AlGaAs wide recess etching stopper 10 and the Si-doped n<sup>+</sup>-type GaAs cap layer 11 can be decreased. That is, a surface potential at the semiconductor surface depletes accumulated electrons in a channel. The increase of the distance between the InGaAs channel layer 5 and the undoped GaAs layer 17 decreases the surface potential effect on the accumulated electrons in the channel. Therefore, the concentration of sheet carriers in the channel is increased by adopting the

undoped AlGaAs layer 16 and the undoped GaAs layer 17.

For example, as illustrated in Fig. 9A, which shows the sheet resistance characteristics where the semiconductor device of Fig. 8 is of an enhancement type having a positive threshold voltage of 0.3V, when a gate recess depth represented by the thickness of the undoped AlGaAs gate recess etching stopper layer 16 and the undoped GaAs layer 17 is more than 5nm, the sheet carrier concentration in the channel is more than  $1 \times 10^{12} \text{ cm}^{-2}$  and the sheet resistance around the wide recess is less than  $1000 \Omega / \square$ . Also, when the gate recess depth represented is 20nm, the sheet carrier concentration in the created channel is  $2.3 \times 10^{12} \text{ cm}^{-2}$  and the sheet resistance around the wide recess is  $450 \Omega / \square$ .

Also, in Fig. 8, since the Schottky barrier is determined by the bandgap of the carbon-doped p<sup>+</sup>-type GaAs layer 15, a high gate breakdown voltage can be maintained even when the carbon-doped p<sup>+</sup>-type GaAs layer 15 is partly buried in the gate recess. Moreover, a reduced parasitic resistance by employing the buried p<sup>+</sup>-type GaAs layer 15 not only reduces the ON-resistance, but also increases a maximum drain current of the device. On the other hand, in Fig 1, the Schottky barrier is determined by both of the AlGaAs Schottky layer 8 and the GaAs layer 9. If the buried amount of the gate electrode 13 is increased, the gate breakdown voltage can be degraded, because a Schottky barrier between GaAs and a gate electrode is 0.3eV lower than that of AlGaAs and a gate electrode. As a result, as illustrated in Fig. 9B, which shows the gate breakdown voltage-to-maximum drain current characteristics, the device of Fig. 8 shows higher maximum drain current and higher gate breakdown voltage than those of the device of Fig. 1.

A method for manufacturing the GaAs heterojunction field effect type semiconductor device of Fig. 8 will be

explained next with reference to Figs. 10A through 10J.

First, referring to Fig. 10A, an about 50nm thick undoped AlGaAs buffer layer 2, an about 4nm thick n<sup>+</sup>-type AlGaAs electron supply layer 3 having about  $3 \times 10^{18}$  Si atoms cm<sup>-3</sup> doped therein, an about 2nm thick undoped AlGaAs spacer layer 4, an about 15nm thick undoped InGaAs channel layer 5, an about 2nm thick undoped AlGaAs spacer layer 6, an about 9nm thick n<sup>+</sup>-type AlGaAs electron supply layer 7 having about  $3 \times 10^{18}$  Si atoms cm<sup>-3</sup> doped therein, an about 7nm thick AlGaAs Schottky layer 8, an about 5nm thick undoped GaAs Schottky layer 9, an about 5nm thick undoped AlGaSAs gate recess etching stopper layer 16, an about 15nm thick GaAs layer 17, an about 5nm thick n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 having about  $4 \times 10^{18}$  Si atoms cm<sup>-3</sup> doped therein and an about 100nm thick n<sup>+</sup>-type GaAs cap layer 11 having  $4 \times 10^{18}$  Si atoms cm<sup>-3</sup> doped therein are sequentially grown on a semi-insulating GaAs substrate 1 by a first epitaxial growth process using an MBE method or an MOVPE method.

Next, referring to Fig. 10B, a photoresist pattern 21 is formed by a photolithography process. Then, the n<sup>+</sup>-type GaAs cap layer 11 is etched by a dry etching process using the photoresist pattern 21 as a mask and the n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 as a stopper. In this case, a part of the n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 is also etched. Thus, a wide recess 11a is created in the n<sup>+</sup>-type GaAs cap layer 11.

Next, referring to Fig. 10C, the remainder of the n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 is completely removed by a rinsing process. Then, the photoresist pattern 21 is removed. Thus, the wide recess 11a is further increased to create a wide recess 10a.

Next, referring to Fig. 10D, an insulating layer 12 made of silicon dioxide is deposited on the entire surface by

a CVD process.

Next, referring to Fig. 10E, a photoresist pattern 22 is formed by a photolithography process. Then, the insulating layer 12 is etched by an etching process using the photoresist pattern 22 as a mask. As a result, the undoped GaAs layer 17 is exposed. Then, the photoresist pattern 22 is removed.

Next, referring to Fig. 10F, the undoped GaAs layer 17 is etched by a dry etching process using the patterned insulating layer 12 as a mask and the undoped AlGaAs gate recess etching stopper layer 16 as a stopper. In this case, a part of the undoped AlGaAs layer 16 is also etched.

Next, referring to Fig. 10G, the remainder of the undoped AlGaAs gate recess etching stopper 16 is completely removed by a rinsing process. Thus, the undoped GaAs Schottky layer 9 is exposed.

Next, referring to Fig. 10H, an about 80nm thick carbon-doped p<sup>+</sup>-type GaAs layer 15 having about  $1 \times 10^{20}$  carbon atoms cm<sup>-3</sup> doped therein is grown on the exposed undoped GaAs Schottky layer 9 by a second epitaxial growth process using an MOVPE method.

Next, referring to Fig. 10I, a gate electrode 13 made of WSi is formed by a sputtering process. Then, the gate electrode 13 is patterned by a photolithography and etching process.

Next, referring to Fig. 10J, the insulating layer 12 is further patterned by a photolithography and etching process. Thus, the n<sup>+</sup>-type GaAs layer 11 is exposed.

Finally, returning to Fig. 8, an ohmic layer made of AuGe is deposited on the exposed n<sup>+</sup>-type GaAs cap layer 11 by an evaporation and lift-off process. Then, the ohmic layer is alloyed and patterned by a photolithography and etching process. Thus, an ohmic source electrode 14S and an ohmic drain

electrode 14D are formed.

In Fig. 11, which illustrates a first modification of the GaAs heterojunction field effect semiconductor device of Fig. 8, the Si-doped n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 of Fig. 8 is replaced by a Si-doped n<sup>+</sup>-type InGaP wide recess etching stopper layer 10'. Even in the GaAs heterojunction field effect semiconductor device of Fig. 11, the gate turn-on voltage V<sub>f</sub> can be increased to about 1.2V. Also, the ON-resistance can be small, i.e., about 1.6Ω · mm.

In Fig. 12, which illustrates a second modification of the GaAs heterojunction field effect semiconductor device of Fig. 8, the Si-doped n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 of Fig. 8 is replaced by a Si-doped n<sup>+</sup>-type InGaP wide recess etching stopper layer 10". The carbon-doped p<sup>+</sup>-type GaAs layer 15 is in contact with the Si-doped n<sup>+</sup>-type InGaP wide recess etching stopper layer 10" that does not include aluminum which is easily oxidized. Even in the GaAs heterojunction field effect semiconductor device of Fig. 12, the gate turn-on voltage V<sub>f</sub> can be increased to about 1.2V.

Also, the ON-resistance can be small, i.e., about 1.6Ω · mm.

When manufacturing the GaAs heterojunction field effect type semiconductor device of Fig. 12, since the complete removing process of the Si-doped n<sup>+</sup>-type InGaP wide recess etching stopper layer 10" is unnecessary, the manufacturing steps therefor can be simplified.

In Fig. 13, which illustrates a third modification of the GaAs heterojunction field effect semiconductor device of Fig. 8, the Si-doped n<sup>+</sup>-type AlGaAs electron supply layer 3, the undoped AlGaAs spacer layers 4 and 6, and the undoped AlGaAs Schottky layer 8 of Fig. 8 are deleted, and the undoped InGaAs channel layer 5 of Fig. 8 is replaced by a Si-doped n<sup>+</sup>-type GaAs channel layer 5'. Even in the GaAs heterojunction field effect semiconductor device of Fig. 13, the gate turn-on

voltage  $V_f$  can be increased to about 1.2V. Also, the ON-resistance can be small, i.e., about  $1.6 \Omega \cdot \text{mm}$ .

When manufacturing the GaAs heterojunction field effect type semiconductor device of Fig. 13, since the layers 5 3, 4, 6 and 8 are unnecessary, the manufacturing steps therefor can be simplified.

In Fig. 14, which illustrates a fourth modification of the GaAs heterojunction field effect semiconductor device of Fig. 8, the carbon-doped p<sup>+</sup>-type GaAs layer 15 of Fig. 8 10 is replaced by a carbon-doped p<sup>+</sup>-type AlGaAs layer 15'.

In the GaAs heterojunction field effect semiconductor device of Fig. 14, the bandgap of AlGaAs is generally larger than that ( $E_g = 1.424\text{eV}$ ) of GaAs. That is, the bandgap  $E_g$  of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  is approximated by

$$\begin{aligned} 15 \quad E_g &= 1.424 + 1.247x \quad (0 \leq x \leq 0.45) \\ &= 1.900 + 0.125x + 0.143x^2 \quad (0.45 \leq x \leq 1.0) \end{aligned}$$

Therefore, if the bandgap of AlGaAs is larger than that of GaAs by about 0.3eV, the effective Schottky barrier is about 1.7eV. As a result, the gate turn-on voltage  $V_f$  can be increased to 20 about 1.5V. Also, the ON-resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D can be small, i.e., about  $1.6 \Omega \cdot \text{mm}$ .

In Fig. 15, which illustrates a fifth modification of the GaAs heterojunction field effect semiconductor device 25 of Fig. 8, the carbon-doped p<sup>+</sup>-type GaAs layer 15 of Fig. 8 is replaced by a carbon-doped p<sup>+</sup>-type InGaP layer 15".

In the GaAs heterojunction field effect semiconductor device of Fig. 15, since the bandgap of InGaP is generally larger than that ( $E_g = 1.424\text{eV}$ ) of GaAs. That is, 30 the bandgap  $E_g$  of InGaP is 1.8 to 1.9eV. If the bandgap of InGaP is larger than that of GaAs by about 0.4eV, the effective Schottky barrier is about 1.8eV. As a result, the gate turn-on voltage  $V_f$  can be increased to about 1.6V. Also, the

ON-resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D can be small, i.e., about  $1.6\Omega \cdot \text{mm}$ .

In Fig. 16, which illustrates a sixth modification 5 of the GaAs heterojunction field effect semiconductor device of Fig. 8, the undoped GaAs Schottky layer 9 of Fig. 8 is replaced by a Si-doped n<sup>+</sup>-type GaAs Schottky layer 9' having about  $5 \times 10^{17} \text{ Si atoms cm}^{-3}$  doped therein.

In the GaAs heterojunction field effect 10 semiconductor device of Fig. 16, since the GaAs Schottky layer 9' is of an n<sup>+</sup>-type, the effective Schottky barrier between the carbon-doped p<sup>+</sup>-type GaAs layer 15 and the Si-doped n<sup>+</sup>-type GaAs Schottky layer 9' is increased, so that the gate turn-on voltage V<sub>f</sub> can be increased to about 1.2V. Also, since the 15 Si-doped n<sup>+</sup>-type GaAs Schottky layer 9' contributes to decrease the contact resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D, the ON-resistance can be small, i.e., about  $1.6\Omega \cdot \text{mm}$ .

In Fig. 17, which illustrates a seventh 20 modification of the GaAs heterojunction field effect semiconductor device of Fig. 8, the undoped AlGaAs layer 16 of Fig. 8 is replaced by a Si-doped n<sup>+</sup>-type AlGaAs layer 16' having about  $5 \times 10^{17} \text{ Si atoms cm}^{-3}$  doped therein.

In the GaAs heterojunction field effect 25 semiconductor device of Fig. 17, since the AlGaAs layer 16' is of an n<sup>+</sup>-type, the effective Schottky barrier between the carbon-doped p<sup>+</sup>-type GaAs layer 15 and the Si-doped n<sup>+</sup>-type AlGaAs layer 16' is increased, so that the gate turn-on voltage V<sub>f</sub> can be increased to about 1.2V. Also, since the Si-doped 30 n<sup>+</sup>-type GaAs layer 6' contributes to decrease the contact resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D, the ON-resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D can be

small, i.e., about  $1.9 \Omega \cdot \text{mm}$ .

In Fig. 18, which illustrates an eighth modification of the GaAs heterojunction field effect semiconductor device of Fig. 8, the Si-doped n<sup>+</sup>-type AlGaAs wide recess etching stopper layer 10 of Fig. 8 is replaced by a Si-doped n<sup>+</sup>-type InGaP wide recess etching stopper layer 10', and the Si-doped n<sup>+</sup>-type GaAs cap layer 11 of Fig. 8 is replaced by a Si-doped n<sup>+</sup>-type In<sub>x</sub>Ga<sub>1-x</sub>As cap layer 11'a having about  $2 \times 10^{19} \text{ Si atoms cm}^{-3}$  doped therein and a Si-doped n<sup>+</sup>-type In<sub>0.5</sub>Ga<sub>0.5</sub>As cap layer 11'b having about  $2 \times 10^{19} \text{ Si atoms cm}^{-3}$  doped therein. Since InGaAs does not lattice match with GaAs, the Si-doped n<sup>+</sup>-type In<sub>x</sub>Ga<sub>1-x</sub>As cap layer 11'a ( $0 \leq x < 0.5$ ) is inserted between the Si-doped n<sup>+</sup>-type InGaP wide recess etching stopper layer 10' and the Si-doped n<sup>+</sup>-type In<sub>0.5</sub>Ga<sub>0.5</sub>As cap layer 11'b.

In the GaAs heterojunction field effect semiconductor device of Fig. 18, the gate turn-on voltage V<sub>f</sub> can be increased to about 1.2V. Also, since the Si-doped n<sup>+</sup>-type InGaAs cap layers 11'a and 11'b contribute to decrease the contact resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D, the ON-resistance between the ohmic source electrode 14S and the ohmic drain electrode 14D can be small, i.e., about  $1.5 \Omega \cdot \text{mm}$ .

The modifications of the second embodiments as illustrated in Figs. 13, 14, 15, 16 and 18 can be applied to the first embodiment of Fig. 4.

In the above-described embodiments, p-type impurities such as Mg or Zn other than carbon can be doped into the p<sup>+</sup>-type GaAs layer 15, the p<sup>+</sup>-type AlGaAs layer 15' or the p<sup>+</sup>-type InGaP layer 15". Also, if the channel layer stores p-type carriers, the GaAs layer 15, the AlGaAs layer 15' and the InGaP layer 15" can be of an n<sup>+</sup>-type.

Further, in the above-described embodiments, the

insulating layer 13 can be made of  $\text{SiN}_x$  or  $\text{SiN}_x\text{O}$

As explained hereinabove, according to the present invention, the gate turn-on voltage  $V_f$  can be increased and the ON current can be decreased.